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An Application-Specific Integrated Circuit (ASIC / ˈ ɛ ɪ ˈ s ɛ ɪ k /) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed to run in a digital voice recorder or a high-efficiency bitcoin miner is an ASIC. Application-specific standard products (ASSPs) are intermediate between ASICs and industry standard ...

Application-specific integrated circuit - Wikipedia

SNUG Boston 2003 Asynchronous & Synchronous Reset Rev 1.3 Design Techniques - Part Deux 2 1.0 Introduction The topic of reset design is surprisingly complex and poorly emphasized.

Asynchronous & Synchronous Reset Design Techniques - Part Deux

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In integrated circuit design, physical design is a step in the standard design cycle which follows after the circuit design. At this step, circuit representations of the components (devices and interconnects) of the design are converted into geometric representations of shapes which, when manufactured in the corresponding layers of materials, will ensure the required functioning of the components.

Physical design (electronics) - Wikipedia

SNUG Boston 2008 Clock Domain Crossing (CDC) Design & Verification Rev 1.0 Techniques Using SystemVerilog 6 1.0 Introduction In 2001, I presented my first paper on multi-asynchronous clock design.

Clock Domain Crossing (CDC) Design & Verification

CIN (RMS) $\| \mathbf{m} \| = \sqrt{\mathbf{m}^T \mathbf{D}^{-1} \mathbf{D} \mathbf{n} \mathbf{m}} = \sqrt{\mathbf{m}^T \mathbf{D}^{-1} \mathbf{m}}$, Advantages of Multiphase Regulators www.ti.com 4 SLVA882 April 2017 Submit Documentation Feedback

Multiphase Buck Design from Start to Finish, Part 1 - TI.com

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Summary: As chip production volumes increases, the per unit cost inevitably goes down. In any one of these categories, the difference in per unit cost between building 10,000 units and 10M units can be anywhere from 2X to 10X.

An Introduction to Semiconductor Economics

Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks Chen Zhang¹
chen.ceca@pku.edu.cn Peng Li² pengli@cs.ucla.edu Guangyu Sun^{1,3} gsun@pku.edu.cn

Optimizing FPGA-based Accelerator Design for Deep

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fsonghan,xyl,huizi,jingpu,perdavan,horowitz,dally@stanford.edu

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