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### **Altium - Wikipedia**

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### **Surprisingly Turing-Complete - Gwern.net**

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### **Cryptocurrency - Wikipedia**

Intel Delays 10-nm Volume Production Until 2019 [https://www.eetimes.com/document.asp?doc\\_id=1333230](https://www.eetimes.com/document.asp?doc_id=1333230). Intel announced the appointment of yet another big-name chip ...

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PLL lock time – Also known as the PLL acquisition time, PLL lock time is the amount of time required by the PLL to attain the target frequency and phase relationship after power-up, after a programmed output frequency change, or after a reset of the PLL. Simulation software does not model a realistic PLL lock time.

### **ALTPLL (Phase-Locked Loop) IP Core User Guide**

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About the Author. Craig Smith (craig@theialabs.com) runs Theia Labs, a security research firm that focuses on security auditing and building hardware and software prototypes. He is also one of the founders of the Hive13 Hackerspace and Open Garages (@OpenGarages). He has worked for several auto manufacturers, where he provided public research on vehicle security and tools.

### **The Car Hacker's™ Handbook - OpenGarages**

Hi, I am using stm32f100rb , and I did configure my clock to 24MHZ, I need help on turning 16 ring rgb WS2812, I am wondering if you could help me , I wrote the code for pwm.

### **Introduction to Microcontrollers - Driving WS2812 RGB LEDs**

Problem 1 sounds more like an idea for a failsafe mechanism to me. If MAX\_INT is, by definition, the maximum amount of reward, then there's no particular reason for the AI to try for MAX\_INT+1.

### **No Time Like The Present For AI Safety Work | Slate Star Codex**

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